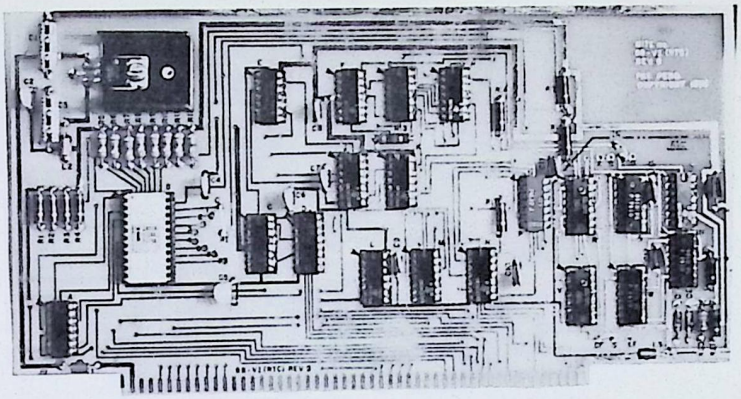
Vector Interrupt / Real Time Clock (88-VI/RTC)



The 88-VI gives the computer the capability to interrupt activity via the Restart (RST) instruction and to allow only the highest active priority of the 8 priority levels to interrupt the CPU.

The Real Time Clock provides the computer user with the capability to interrupt the processor at one of four selectable rates. The RTC generates an interrupt after a precise interval of time, which enables software to time certain routines and even to generate the correct time, day, and year, upon request.

The RTC source may be selected from either a derivative of the 2 megahertz clock or the line frequency. The 2 megahertz clock should be used if a fast RTC is needed; it is selectable for time intervals down to every 100 microseconds. The line frequency (60 Hertz) should be used in systems that require accuracy over a long period of time.

Hardware

Altair Slots: One.
Power: 5 volts at 300 ma.

Operation

ENABLE INTERRUPT instruction of the computer permits interruption. ENABLE INTERRUPT must also be activated after each interrupt is completed in order to reactivate the CPU's internal interrupt.

RST is an instruction which translates in octal code to 3N7; where "N" is a 3 bit code which represents one of the 8 priority locations, 0, 10, 20, 30, 40, 50, 60, or 70 (octal). Restart instructions are RST0= 307, RST10= 317, RST20= 327, etc. (octal). The vector interrupt places the RST instruction on the data bus at the correct time.

The 88-VI directs the interrupt to one of its 8 bus lines (VI0-VI7). VI0 is the highest priority, VI7 is the lowest.

The RST address will direct the computer to the highest active VI bus line. When an interrupt occurs that is higher priority than the active interrupt, the 88-VI interrupts the CPU and puts the RST instruction and the 3-bit address associated with that priority level on the data bus.

The Interrupt Service Handler is the software device which supervises all individual device service routines. Interrupt Service Handler enables the interruption of a lower interrupt routine by a higher one and also insures that each lower routine will be returned to and fully executed.

Address: Address 376 (octal). Bits 0, 1, 2, and 3 are used to update current level status. Bit 6 is used to enable/ disable the Vector Interrupt feature.

The Real Time Clock offers 2 clock sources: the system clock (operates at 2 megahertz), or the line frequency (operates at 60 hertz). The system clock interrupts once every 100 microseconds, 1 millisecond, 10 milliseconds, or 100 milliseconds. Line frequency interrupts once every 16.67 milliseconds, 166.7 milliseconds, 1.667 seconds, or 16.07 seconds. Any of the selected time intervals may be used to interrupt at any one of the 8 priority levels.

Clock Source Intervals:
System Clock [2MHz]: 100 ns, 1 ms, 10 ms, or 100 ms.

Line Frequency [60Hz] Intervals: 16.67 ms, 166.7 ms, 1.667 sec., or 16.67 sec.

Accuracy: 2MHz, .01%.

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